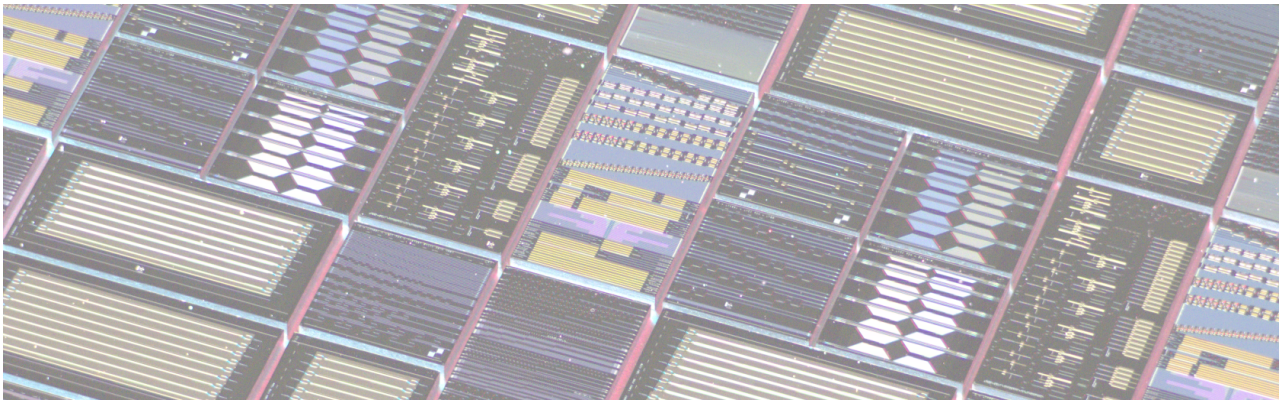
Luxtelligence SA
EPFL Innovation Park
foundry@luxtelligence.ai

Design manual for PIC fabrication with Luxtelligence

Luxtelligence SA (LXT) is a photonics foundry specialized in the microfabrication of integrated optical components in ferroelectric materials, which can be modulated and configured by the application of electric fields.



1 Versions of this document

- **1.4**: Fix an error in the definition of layer 3/0.
- **1.3**: Add some material properties and introduce the use of layer 2/1.
- **1.2**: Add a section documenting common design mistakes.
- **1.1**: Include a plot displaying the refractive index of LN.
- **1.0**: First release of the Luxtelligence design manual, including information on multi-project wafer runs: typical MPW timeline, current MPW cross-section, PDK access and design rules.

2 Terms and conditions

To partake in a fabrication project, customers must agree with the general terms and conditions shared by Luxtelligence upon sales contact. The email address foundry@luxtelligence.ai can be used for inquiries about participation in a scheduled fabrication run or collaboration on a custom project. Please note that our provided delivery dates are estimates and are not binding. We are not to be held liable for any delays that are beyond our control and are the responsibility of our service providers, for example in the case of cleanroom shutdowns, unforeseen maintenance, delays in handling by the packaging partners.

3 Introduction

Luxtelligence provides services of fabrication of custom photonic integrated circuits with thin film lithium niobate as a waveguiding material. Lithium niobate is an attractive material for integrated photonics, due to its almost perfect transparency at optical and infrared wavelengths, and to a sizeable electro-optic effect, that permits active modulation with the application of local electric fields.

Author: design@luxtelligence.ai
Title: LXT design manual
Category: Technical report - confidential
Date: March 21, 2025
Version: 1.3
Status: Released

This feature allows, for example, the construction of phase and amplitude modulators, tunable filters and interferometers. In addition, nonlinear devices, for second harmonic generation, frequency conversion, production of highly-correlated light states, can be implemented, exploiting the material's second order optical susceptibility.

We help our customers realize their integrated optical prototype by offering both Multi-Project Wafers (MPWs) and custom fabrication runs. In the MPW runs, a design space is shared between several designers, to reduce the cost-per-die, and the cross-sectional geometry is chosen to ensure an ample design flexibility, and kept fixed to guarantee reproducibility and a good control of the process. In custom runs, customers have large margins of freedom in the choice of film thicknesses, electrode location and thickness and etch processes, which are defined together with the LXT team according to criteria of technical and economic feasibility. On the other hand, since the design space is attributed to one or few customers, the final price per run is higher than for MPWs.

Microfabrication is a complex discipline, where empirical details of seemingly negligible effect are actually crucial to the performance of the desired devices. To improve the quality and consistency of the PIC fabrication process, and avoid unexpected results, some design rules, related to the fabrication methods, are enforced before the layout acceptance. In this design manual, we describe these design rules, with particular focus on MPW runs. The design rules can be interpreted as approximate guidelines also for custom fabrication runs, although in this case they could be adapted to ensure pattern fidelity on a different material stack or relaxed, since looser yield criteria are acceptable.

Glossary of common acronyms

- DRC: Design Rule Check
- GDS (GDSII): Graphic Design System. A common file format for sharing planar circuit layouts (both photonic and electronic components), in the form of polygons and traces
- LN: Lithium Niobate, $LiNbO_3$
- LNOI: Lithium Niobate on Insulator
- MPW: Multi-Project Wafer
- NRE: Non-Recurring Engineering
- PIC: Photonic Integrated Circuit
- PCM: Process Control Monitoring
- PDK: Process Design Kit

4 Multi-project wafers

Submitting for an MPW run with Luxtelligence

MPW runs start multiple times during the year. You can find a calendar with the upcoming submission deadlines on our website, and inquire about participation by contacting foundry@luxtelligence.ai. The typical customer timeline for an MPW participation is sketched in Fig. 1. Our PDK is readily available from multiple sources (see the relevant section), and design can start at any point in time

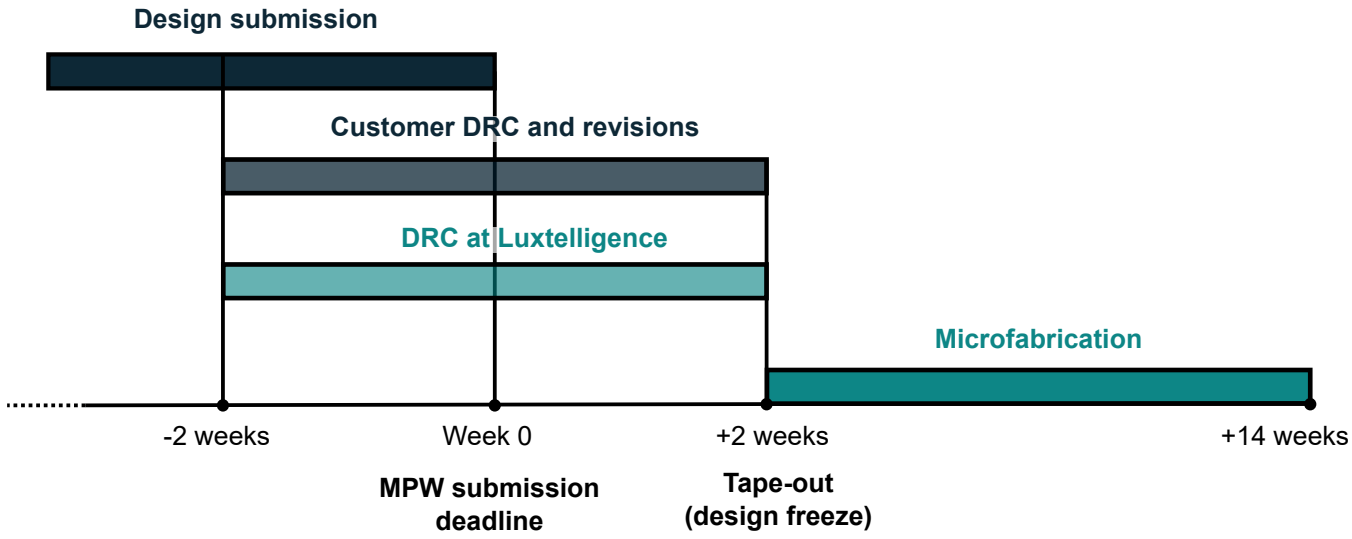


Figure 1: *Standard timeline for tape-out, design rule checking (DRC) and fabrication for MPW runs at Luxtelligence.*

using the PDK elements or the customer-defined building blocks. We then carry out an inspection and design rule check (DRC) procedure alongside the customer, accepting preliminary designs starting two weeks before the submission deadline. The DRC consists both of detailed inspection by our fabrication and design engineers, as well as automatized routines running on the GDS layout, that assess the rules specified in the following sections. We recommend using the layout viewer K-Layout for quick and accurate mask inspection. The DRC will carry on until two weeks after the submission deadline; generally 2-5 design iterations are necessary before finalizing a satisfactory design that passes the DRC. Until two weeks after the deadline, customers can also add or change elements in their layouts. Two weeks after the submission deadline, we will proceed with the tape-out. The designs will be frozen and no more modifications or DRC iterations are carried out; the process masks will be finalized and fabricated at once, such that no more changes are possible. The microfabrication at LXT will then start, with delivery of the final dies expected typically 12 weeks after tape-out (excluding holidays), provided no major equipment faults, unforeseen maintenance or supplier delays.

Cross sectional layout for MPW runs

For MPW runs, we utilize x-cut LNOI wafers (see Fig. 2): the single crystalline LN crystal is grown, cut, and bonded on the carrier wafer such that the x crystalline axis is normal to the wafer surface. [1]. In this configuration, the strongest phase modulation (electro-optical tensor component $r_{33} = 30\,\mathrm{pm/V}$) can be obtained with waveguides oriented along the y direction, the electric field polarization oriented along z (waveguide TE mode), and symmetric electrode placement like the illustration in Fig. 2. In MPW designs, we assume the horizontal direction to be y and the vertical direction to be z: modulator waveguides should run horizontal.

The MPW fabrication process utilizes two masks for optical components, and one mask layer for electrical components, such as microwave transmission lines and heaters. The material cross-section used for the MPW runs is portrayed in Fig. 2, with relevant geometric dimensions indicated.

[1] Lithium niobate is a crystal with uniaxial birefringence: the x- and y- axes are ordinary while the z axis is extraordinary and is associated to a lower refractive index.

The starting LN thickness is 400 nm, and LN is separated from the silicon substrate by a buried oxide layer (SiO_2) ($t_{BOX} = 4.7\,\mu m$). Waveguides are defined by partially etching ridges into the lithium niobate film ($t_{ridge} \approx t_{slab} \approx 200\,nm$, typical uniformity on the wafer around 5%). Etched ridge sidewalls are quasi-vertical, typically oriented between $75 - 78^\circ$ from the slab surface. The second optical etch step removes the remaining LN slab in selected regions, generally with the goal of defining bilayer edge couplers (refer to the distributed PDK). A silicon oxide cladding is deposited on the LN waveguides, with a thickness of $t_{TC} \approx 2.0\,\mu m$. Gold electrodes with a thickness of $t_{el} = 900\,nm$ are fabricated inside a recess in the top cladding. A vertical offset of $t_{EO} = 1.0\,\mu m$ separates the top of the optical waveguides from the bottom surface of the electrodes.

Material properties

The ordinary and extraordinary refractive indices of a bulk Lithium Niobate crystal (congruent growth) are shown in Fig. 3. For the optical designers who desire to model the optical dispersion of Lithium Niobate, we provide here the coefficients of a Sellmeier fit to experimental data. The Sellmeier equation for the refractive index dispersion is:

$$n(\lambda) = \sqrt{\epsilon_\infty + \frac{A\lambda^2}{\lambda^2 - B^2}}, \tag{1}$$

and the fit coefficients are provided in Table 1.

	A	B	ϵ_∞
n_o	3.0	0.20315	1.834
n_e	2.0	0.21738	2.513

Table 1: *Sellmeier coefficients for the ordinary and extraordinary indices of thin film lithium niobate.*

The effective and group indices for various waveguide widths and propagation along the y direction (with TE polarization, TE_{00} mode) have been simulated, and the results are shown in Fig. 4. The RF behaviour of the material stack is well approximated by literature values for the Lithium Niobate relative permittivity; $\epsilon_{xx,yy} \approx 38, \epsilon_{zz} \approx 28$.

For the gold layer of Fig. 2, the sheet resistance is estimated to be about 0.035 Ohm/sqr.

Process design kit

A process design kit for the MPW fabrication stack is freely available for download from the Luxtelligence website. It is currently implemented in the photonic design tools IPKISS and gdsfactory, where the component layouts are made available, alongside netlists and circuit models that approximate their dispersive behaviour. The PDK consists of crucial passive and active building blocks for building electro-optical modulators in the infrared C-band (around 1550 nm), relevant for optical communications. Both optical and microwave waveguide templates and components are available, and layout cells can be parametrized according to the designer's needs. Note that the IPKISS PDK contains a *virtual fabrication* function, such that cross section views like Fig. 2 can be generated at arbitrary lines in the layout.

Please be aware that, although our code is open source, using the IPKISS design platform requires a paid or trial license. Contact support@lucedaphotonics.com for assistance in obtaining a license suitable to your needs.

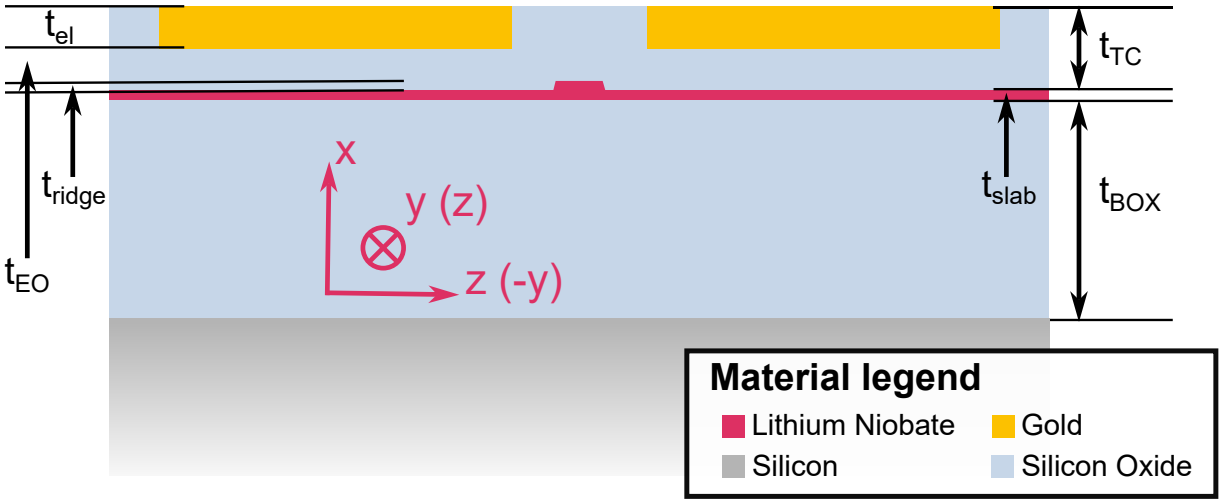


Figure 2: *Cross-sectional view of the material stack for multi-project wafers, including the waveguide, cladding and electrode layers. The relevant film thickness parameters are marked. The orientation of the crystal axes of lithium niobate is described by the magenta Cartesian axes.*

Layers and design rules

The design rules described in this section are meant to guarantee fabrication yield and quality, and their compliance is checked during the joint LXT-customer DRC process. The fabrication layout is defined by different layers of traces and shapes, corresponding to different layers in the GDS file. Each layer corresponds to the combination of a fabrication step and a pattern purpose, so that the number of GDS layers is higher than the patterning steps in the fabrication process. Boolean operations between layers, and layer merging are performed digitally by the LXT team before the process masks fabrication. The layer numbers are defined in Table 2. A set of layout properties for K-Layout is distributed with the PDK, facilitating the visualization with a high contrast color palette.

Die size

The allowed die dimensions are combinations of 5.05 mm, 10.1 mm, 20.2 mm, with a minimum die size of 5.05 mm × 10.1 mm. We define a 50 µm-wide area around the edges of all chips as an *exclusion zone*. No components can intersect this area, except for edge couplers that route to the chip facets. This convention is enforced to obtain a consistent quality of the die singulation process, and to avoid device degradation from simple chip handling. In addition, square areas of size 75 µm × 75 µm close to the chip corners should be left free, as they are reserved for foundry structures necessary to the fabrication process.

In our PDK distribution, the chip frame is drawn on GDS layer 6/1 and the "usable floorplan area" (after subtraction of the exclusion zone) is drawn on layer 6/0 (see Fig. 5). The dicing lines coincide with the edges of the rectangle on layer 6/1.

LN etch (ridge)

Layer 2/0 contains the waveguides and photonic devices to be partially etched in the LN film (200 nm depth). The polygons on this layer define a **light field mask**: the areas inside the polygons

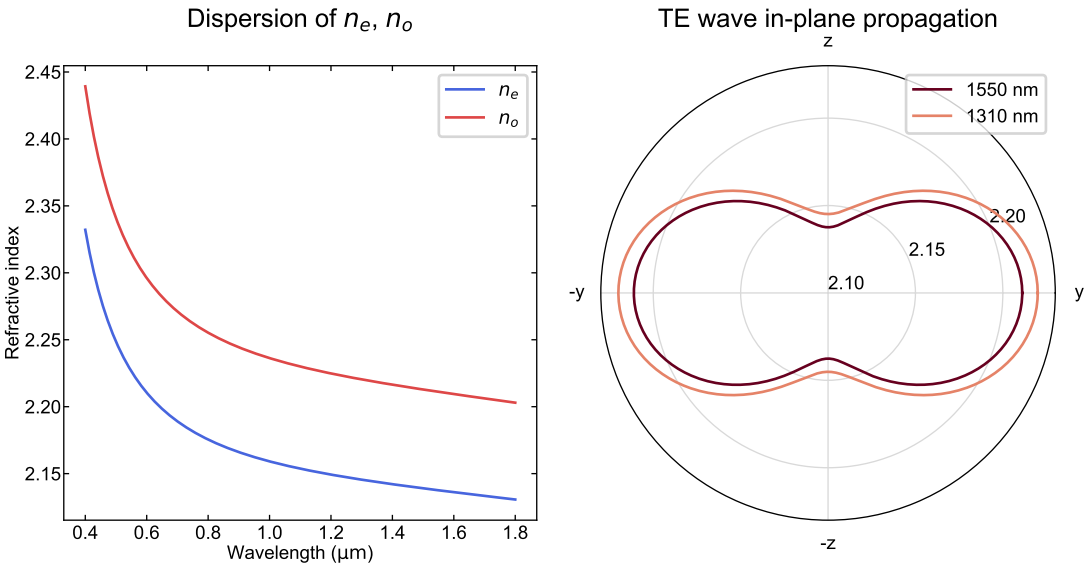


Figure 3: *Birefringent properties of bulk lithium niobate. Left: wavelength dispersion of the ordinary and extraordinary indices. Right: refractive index of a TE-polarized wave propagating in the yz plane. The z-direction coincides with the optical axis.*

correspond to protected regions in the thin film that will not get etched in the patterning process. In this layer, the minimum accepted feature width for isolated patterns (waveguides) is 250 nm. The minimum gap between features should be no smaller than 300 nm. Refer to the illustration in Fig. 6

For the **discretization of waveguide bends**, a distance of 500 nm between adjacent vertices is recommended. Given the typical bending radii of > 45 µm, this already translates in less than 2 nm

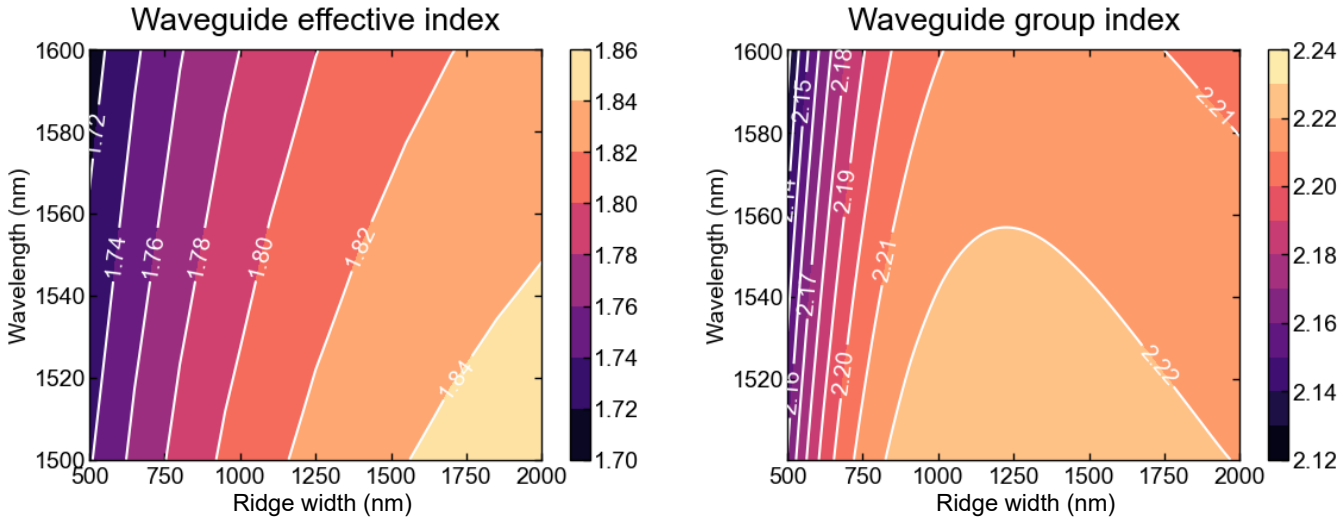


Figure 4: *Simulated waveguide effective index (left) and group index (right) for different wavelengths and ridge widths in the MPW material stack portrayed in Fig. 2.*

Pattern and purpose	GDS layer	Field	Min. feature size (nm)	Min. gap (nm)
LN etch (ridge)	2/0	Light	250	300
LN etch (ridge, periodic features)	2/1	Light	250	300
LN etch (full)	3/0	Light	250	-
Slab etch negative	3/1	Dark	-	250
Labels (LN etch)	4/0	Light	250	300
Alignment markers (LN etch)	31/0	Light	250	300
Metal transmission lines	21/0	Light	800	1000
Metal heaters	21/1	Light	800	1000
Usable floorplan area	6/0	-	-	-
Final chip boundaries	6/1	-	-	-

Table 2: *Summary table of the GDS layers used for defining fabrication patterns and of the minimum feature sizes accepted for MPW fabrication. A light field mask is defined as a mask where the interior of the drawn polygons is preserved in the patterned thin film and the exterior is removed, irrespective of the lithography tone. Vice-versa for a dark field mask.*

deviation from the perfectly smooth circle. An even finer discretization would yield no benefit and would only increase the file size and computational load necessary to process the masks.

We strongly recommend our customers to place on **layer 2/1** small, repeating features in the LN ridge etch layer, such as those that define a photonic crystal or a Bragg reflector (see Fig. 7). This will greatly facilitate the process of DRC and reticle assembly, and reduce the probability of a mask handling error.

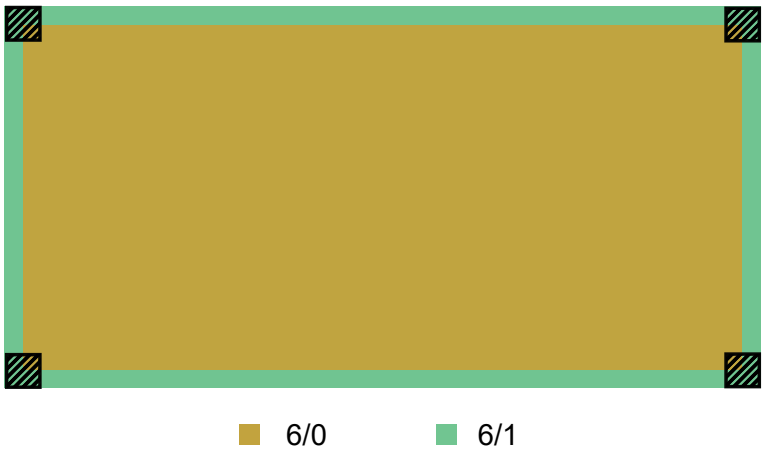


Figure 5: *Visualization of the chip frame on the respective GDS layers. The areas in the green rectangle but not in the ochre rectangle should be left free of components except edge couplers. The hatched areas at the corners should be left completely free.*

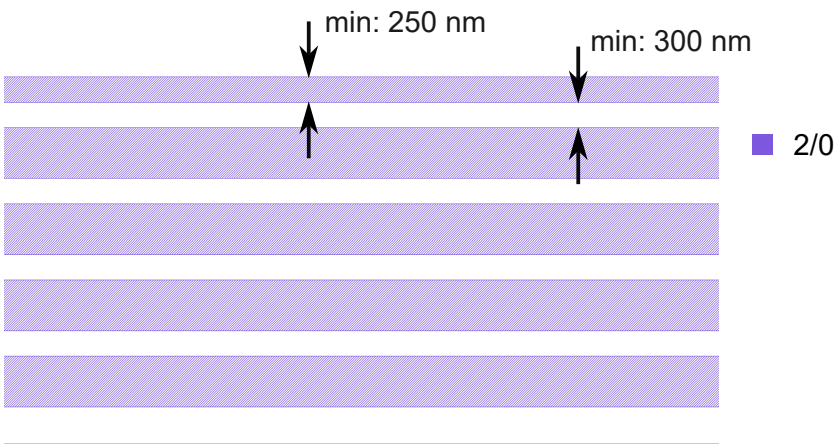


Figure 6: *Ridge etch pattern on layer 2/0. The minimum acceptable positive and negative feature widths are marked on the illustration.*

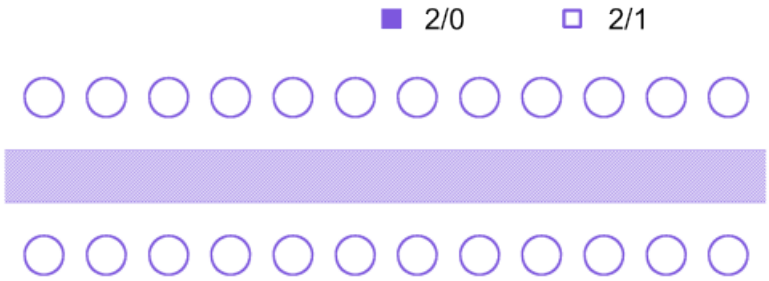


Figure 7: *Layer 2/0 is used to define ridge waveguide profiles, while large arrays of periodic structures should be placed on layer 2/1.*

LN etch (full)

Layer 3/0 contains the areas where the LN slab will be patterned on the wafer. The polygons on this layer define a **light field mask**: the areas inside the polygons correspond to protected regions in the thin film that will not get etched in the patterning process. In MPW runs, this layer is mostly used for the definition of bilayer edge couplers: for the rib waveguides used in routing, it is not necessary to pattern the slab. In our PDK distributions, however, the slab around rib waveguides is shown on 3/0 despite not being patterned. In this layer, the minimum accepted feature width for isolated patterns (waveguides) is 250 nm. Refer to the illustration in Fig. 8

Slab etch mask

Layer 3/1 is used to draw the negative of the slab etch patterns of layer 3/0, which is needed in order to fabricate the process masks. The polygons on this layer define then a **dark field mask**: the areas inside the polygons correspond to regions in the thin film that will get etched in the patterning process. Features on layer 3/1 are typically located close to the chip edges, where the LN slab needs to be removed to define edge coupler components (see Fig. 9 for an example of correct edge coupler

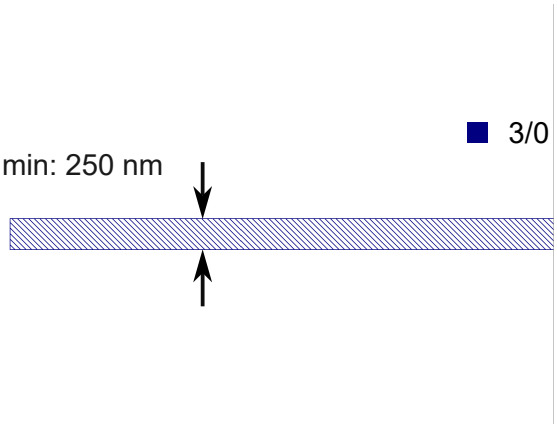


Figure 8: *Slab etch pattern on layer 3/0. The hatched area on layer 3/0 will be retained in the LN thin film after patterning.*

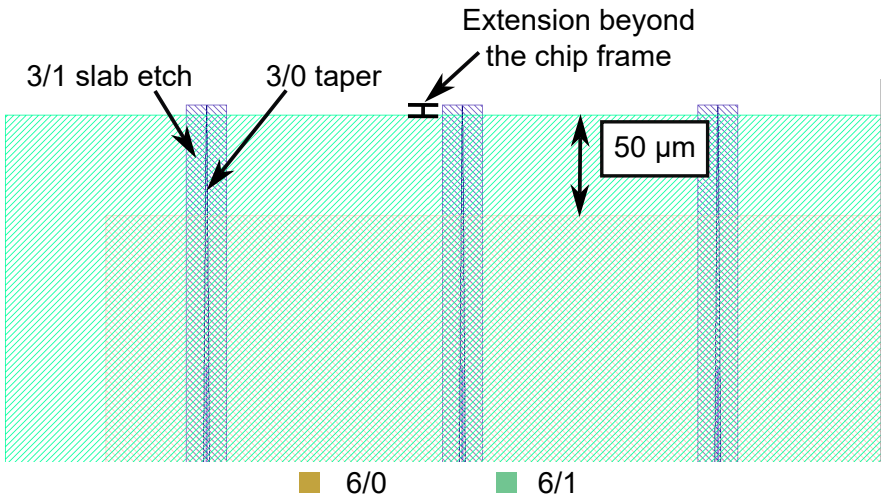


Figure 9: *Illustration of the placement specifications for edge couplers. Relevant layout utilities are distributed with the PDK.*

placement on the chip frame).

The fabrication mask for the second etch will be created at Luxtelligence starting from the customer layouts by performing the boolean operation 3/1 MINUS 3/0.

Metal transmission lines and heaters

Layers 21/0 and 21/1 are used respectively for the definition of gold RF transmission lines and heaters for phase tuning through the thermo-optical effect. The polygons on this layer define a **light field mask**: the areas inside the polygons correspond to protected regions in the thin film that will not get etched in the patterning process. At the moment, heater and transmission line structures are patterned in the same thin film; see the cross section portrayed in Fig. 2. In these layers, the minimum accepted feature width for isolated patterns (e.g. heater lines) is 800 nm. The minimum gap between features should be no smaller than 1000 nm. Refer to the illustration in Fig. 10.

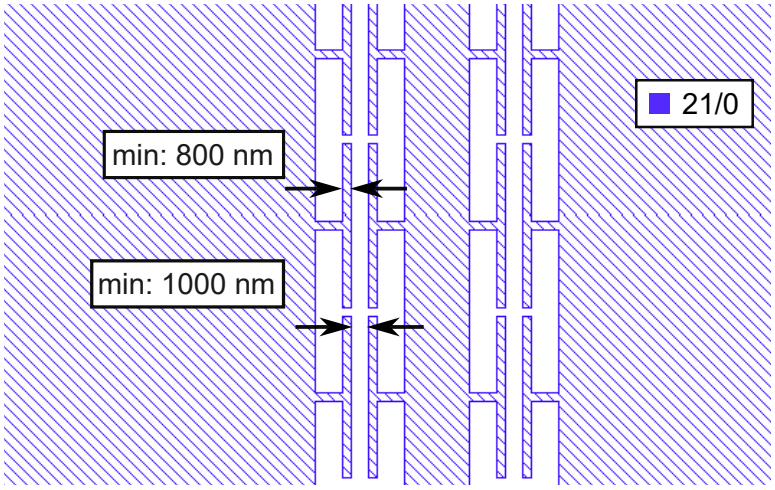


Figure 10: *Transmission line pattern on layer 21/0. The minimum acceptable positive and negative feature widths are marked on the illustration.*

Labels and alignment markers

Layers 4/0 and 31/0 are used respectively for the definition of labels and alignment markers patterned as LN ridges. The polygons on this layer define a **light field mask**: the areas inside the polygons correspond to protected regions in the thin film that will not get etched in the patterning process. The fabrication mask for the first etch will be created at Luxtelligence starting from the customer layouts by performing the boolean operation 2/0 PLUS 4/0 PLUS 31/0. Nevertheless, labels and alignment markers should be placed on different layers from optical devices due to different dimensional and lithographic requirements. Labels cannot be patterned in metal, as this could compromise the behaviour of adjacent structures. It is recommended to keep labels and markers separated by a distance of at least 12 µm from any wave-guiding structures.

Filler pattern and guard-rails

During the mask fabrication, Luxtelligence will add some filler pattern structures in any large empty areas devoid of any structures. The filler pattern is defined in the ridge etch step. We will ensure that these structures do not intersect with any features on the photonics or metal layers. In addition, in order to maximize the consistency of exposure conditions along the waveguides, "guard-rail" structures will be added if necessary. These guard-rails are simply dummy waveguides that run parallel to the device waveguides. They are only added along isolated waveguides, and they are also interrupted if they would intersect with any LN etch or metal layers. See Fig. 11 for an example of filler pattern and guard-rails.

Quality assessment

Each MPW run is validated at LXT, both during the fabrication process, with appropriate metrology steps, and after the fabrication process, by testing Process Control Monitoring (PCM) devices. Standard PCM structures are included on all the MPW wafers, in a design area separated from the customer chips. These “sentinel” devices are meant to provide tangible and easily-accessed information on the quality of the fabrication run, and to guarantee that the electrical and optical performance parameters crucial to the operation of the PICs lie within a reasonable range. At the moment, the

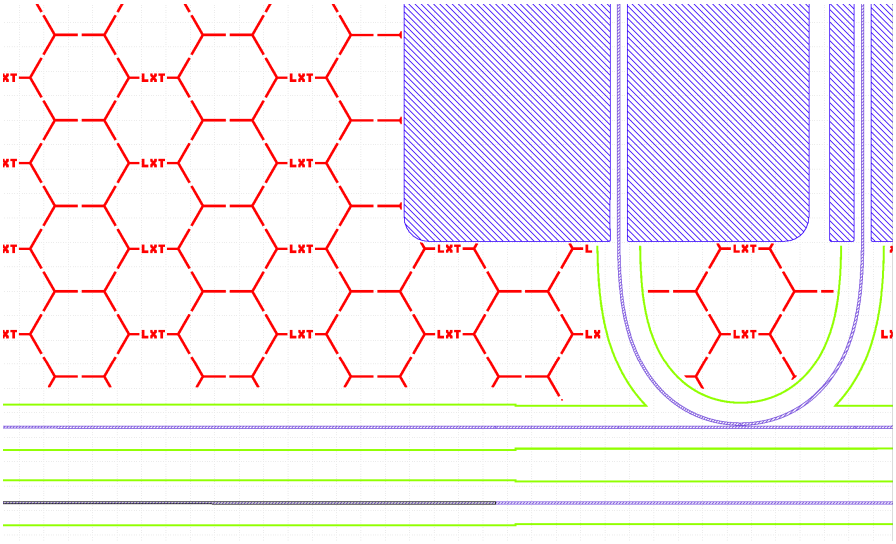


Figure 11: *Filler pattern structures (red) and waveguide guard-rails (green) around the device structures (purple). Note that these additional structures are excluded from metal layers to avoid generating topography in the electrodes.*

PCM device	Specifications	Figure of merit	Worst-case performance
Ring resonator	200 µm radius, 1550 nm, TE pol.	Intrinsic Q	$> 1.5 \cdot 10^5$ (~ 2.5 dB/cm)
MZ modulator	1550 nm	$V_\pi \times L$ (at 1 MHz)	< 5 V cm

Table 3: *PCM structures included in MPW runs, and their key metrics that are characterized after microfabrication. Q indicates the resonator quality factor, TE the transverse-electric polarization and V_π the voltage swing necessary for inducing a phase shift of π at the specified ramp frequency.*

PCM components include ring resonators and Mach-Zehnder modulators, and their measured performance metrics are specified in Table 3. The MPW yield is considered acceptable if the distribution of the performance in the specified figures of merit is such that more than 90% of the devices fulfill or improve on the worst-case performance in the table. Note that the worst-case performance is significantly worse than the typical measured parameter's of the PCM devices.

Common design pitfalls

Here we list some of the most frequent layout errors that are addressed during DRC.

- **Incorrect die dimensions.**

  The allowed die dimensions can be chosen among 5.05 mm, 10.1 mm, 20.2 mm, to maintain compatibility with the reticle assembly. Slightly different die sizes will hinder the mask set assembly process and compromise the definition of fiber coupling structures.

- **Incorrect instance orientation.**

  Lithium niobate is a birefringent material (see Fig. 3). That means that the orientation of PDK components is important and should not be manipulated without taking into account the change of refractive indices. In particular, electro-optic modulation sections should be **horizontally-aligned** in the mask delivered to LXT, for the best modulation efficiency (see Fig. 12).

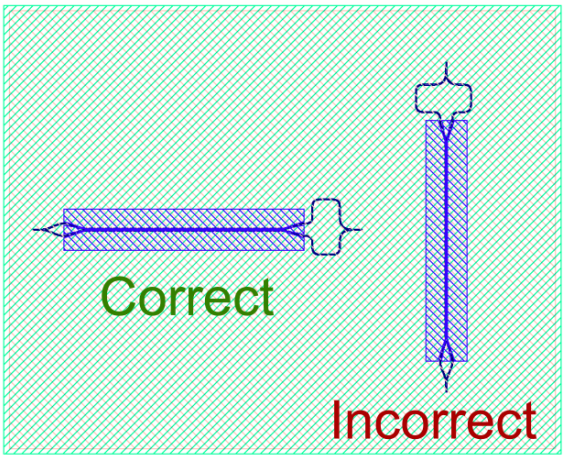


Figure 12: *Examples of correct and incorrect orientation of a Mach-Zehnder modulator.*

- **Imprecise edge couplers positioning.**

  The exact placement of edge couplers is crucial for their proper operation. The coupler waveguide should **protrude from layer 6/1** of about 5 µm to account for chip singulation tolerances. At the same time, it is recommended to extend the edge coupler with a short uniform-width waveguide, about 10 µm long, **whose midpoint is placed on the edge of the 6/1 box**. This reduces the sensitivity of the facet cross-section geometry to small alignment errors in the chip singulation step. Please refer to the examples shown in Fig. 13.

  In case of subsequent chip facet polishing (not offered for MPW runs), the uniform extension should be made appropriately longer, according to the polishing specifications.

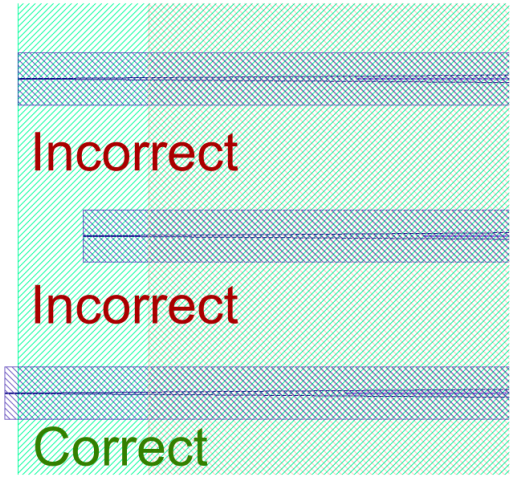


Figure 13: *Examples of correct and incorrect placement of edge couplers at the die boundary.*

- **Insufficient bend segmentation.**

  Waveguide bends should be discretized with a sufficient resolution, to avoid unnecessary optical losses coming from a rough polygon segmentation. We recommend a discretization step of 500 nm for the wavelength of 1550 nm.